

**What Is Claimed Is:**

1        1. A method for fabricating a liquid crystal display  
2 including a plurality of pixels, the method comprising the steps  
3 of:  
4              forming a gate pattern, including a plurality of separated  
5                  gate lines and a gate electrode array electrically  
6                  connected with the separated gate lines, in a  
7                  substrate;  
8              forming a channel array, isolated from the gate electrode  
9                  array;  
10          forming a source/drain pair array, with the source and  
11                  drain spaced apart from each other, in the channel  
12                  array; and  
13          forming a pixel electrode array to connect the drains of  
14                  the source/drain pair array;  
15          wherein the steps for forming the gate pattern or the  
16                  source/drain pair array, at least, comprise the steps  
17                  of:  
18              forming a photoresist layer;  
19              dividing the photoresist layer into a first region, a  
20                  second region, and a boundary region, divided into  
21                  a first portion and a second portion by a boundary  
22                  line, between the first region and the second region;  
23          defining the first region and the first portion with a first  
24                  mask; and  
25          defining the second region and the second portion with a  
26                  second mask;  
27          wherein the boundary region corresponds to a sub-array of  
28                  the gate electrode array or the source/drain pair

29               array; for each row of the gate electrodes or each  
30               row of the source/drain pairs in the sub-array, the  
31               boundary line is formed in a special pattern; the  
32               gate electrodes or the source/drain electrode pairs  
33               at the boundary region defined by both of the first  
34               and second masks are divided into a first portion  
35               patterned by the first mask and a second portion  
36               patterned by the second mask; the boundary region is  
37               divided incrementally or by square wave such that the  
38               area of each of the gate electrodes or the  
39               source/drain electrode pairs in the first portion  
40               increases along the boundary direction and that in  
41               the second portion decreases along the boundary  
42               direction.

1               2. The method as claimed in claim 1, wherein the boundary  
2               line used for dividing each row of the gate electrodes and each  
3               row of the source/drain pairs is a tilted straight line.

1               3. The method as claimed in claim 1, wherein the boundary  
2               line used for dividing each row of the gate electrodes and each  
3               row of the source/drain pairs is in a ladder pattern.

1               4. The method as claimed in claim 1, wherein the boundary  
2               line used for dividing each row of the gate electrodes and each  
3               row of the source/drain pairs is in a square wave pattern.

1               5. The method as claimed in claim 1, wherein the boundary  
2               line used for dividing each row of the gate electrodes and each  
3               row of the source/drain pairs is in an embedded line pattern.

1       6. The method as claimed in claim 1, wherein the boundary  
2 line divides a row of the gate or source/drain electrodes from  
3 the first region to the second region, then continues to divide  
4 the next row of the gate or source/drain electrodes from the  
5 second region to the first region, and so forth.

1       7. The method as claimed in claim 1, wherein the boundary  
2 line divides a row of the gate or source/drain electrodes from  
3 the first region to the second region, then goes back to the first  
4 region and continues to divide the next row of the gate or  
5 source/drain electrodes from the first region to the second  
6 region, and so forth.

1       8. A liquid crystal display, wherein the shot mura  
2 phenomenon is minimized, is fabricated with the method as  
3 claimed in claim 1.

1       9. A method for fabricating a liquid crystal display  
2 including a plurality of pixels, the method comprising the steps  
3 of:

4             forming a gate pattern, a gate electrode array , a channel  
5             array isolated from the gate electrode array, a  
6             source/drain pair array, and a pixel electrode array  
7             in a substrate; wherein the gate pattern includes a  
8             plurality of separated gate lines connected with the  
9             electrode array, and the source and drain in each  
10            source/drain pair are spaced from each other, and the  
11            pixel electrode array is coupled to the drains of the  
12            source/drain pair array;

13       and wherein the steps for forming the gate pattern and the  
14                  source/drain pair array, at least, comprise the steps  
15                  of:  
16                  forming a photoresist layer;  
17                  dividing the photoresist layer into a first region, a  
18                          second region, and a boundary region, divided into  
19                          a first portion and a second portion by a boundary  
20                          line, between the first region and the second region;  
21                  defining the first region and the first portion with a first  
22                          mask; and  
23                  defining the second region and the second portion with a  
24                          second mask;  
25                  wherein the boundary region corresponds to a sub-array of  
26                          the gate electrode array or the source/drain pair  
27                          array; for each row of the gate electrodes or each  
28                          row of the source/drain pairs in the sub-array, the  
29                          boundary line is formed in a special pattern; the  
30                          gate electrodes or the source/drain electrode pairs  
31                          at the boundary region defined by both of the first  
32                          and second masks are divided into a first portion  
33                          patterned by the first mask and a second portion  
34                          patterned by the second mask; the boundary region is  
35                          divided incrementally or by square wave such that the  
36                          area of each of the gate electrodes or the  
37                          source/drain electrode pairs in the first portion  
38                          increases along the boundary direction and those in  
39                          the second portion decreases along the boundary  
40                          direction.

1       10. The method as claimed in claim 9, wherein the boundary  
2 line used for dividing each row of the gate electrodes and each  
3 row of the source/drain pairs is a tilted straight line.

1       11. The method as claimed in claim 9, wherein the boundary  
2 line used for dividing each row of the gate electrodes and each  
3 row of the source/drain pairs is in a ladder pattern.

1       12. The method as claimed in claim 9, wherein the boundary  
2 line used for dividing each row of the gate electrodes and each  
3 row of the source/drain pairs is in a square wave pattern.

1       13. The method as claimed in claim 9, wherein the boundary  
2 line used for dividing each row of the gate electrodes and each  
3 row of the source/drain pairs is in an embedded line pattern.

1       14. The method as claimed in claim 9, wherein the boundary  
2 line divides a row of the gate or source/drain electrodes from  
3 the first region to the second region, then continues to divide  
4 the next row of the gate or source/drain electrodes from the  
5 second region to the first region, and so forth.

1       15. The method as claimed in claim 9, wherein the boundary  
2 line divides a row of the gate or source/drain electrodes from  
3 the first region to the second region, then goes back to the first  
4 region and continues to divide the next row of the gate or  
5 source/drain electrodes from the first region to the second  
6 region, and so forth.